DSG-NPS R&D Meeting Minutes

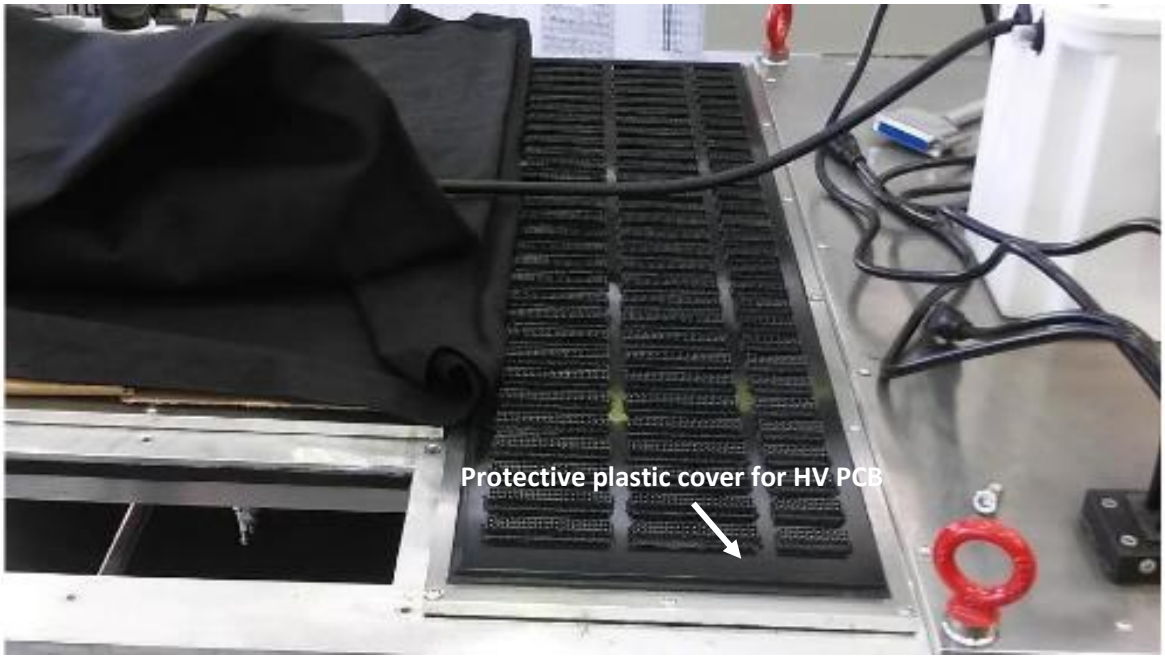
Date: March 16, 2021
Time: 11:00AM – 12:30 PM

Attendees: Mary Ann Antonioli, Peter Bonneau, Aaron Brown, Pablo Campero, Brian Eng, George Jacobs, Mindy Leffel, Tyler Lemon, Marc McMullen, and Amrit Yegneswaran

1. HV supply cable fabrication and testing

Peter Bonneau, Aaron Brown, Brian Eng, George Jacobs, Mindy Leffel, and Marc McMullen

1. SAMTEC, 8-pin, board-mount connectors (25 pcs) arrived; 15-pin, board-mount connectors scheduled to arrive on 03/17/2021
2. Reviewed procedure for HV supply cable testing
   - Voltage will be ramped from 0 V to 1200 V to 2400 V
   - Ramp rate will be set to 250 V/s
   - George Jacobs will conduct test and monitor cable and connectors
3. Discussed protective covering for HV PCB; reviewed photo of detector from IPN Orsay showing HV PCB with plastic covering in place in detector frame



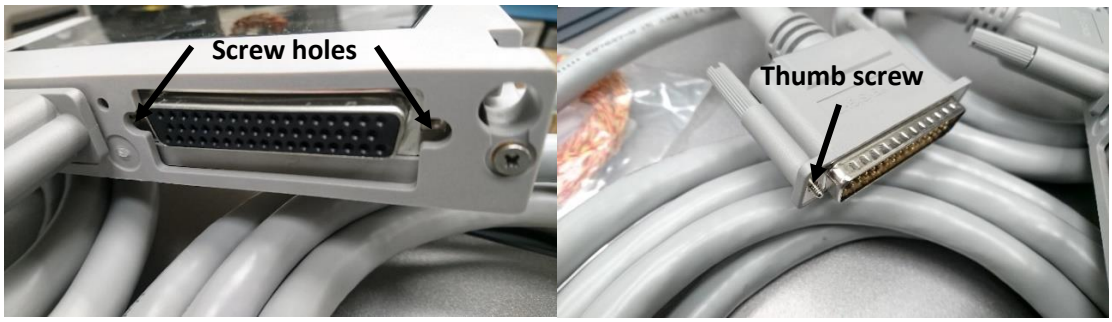
High voltage PCB installed in NPS detector frame with plastic protective cover

4. SAMTEC connector PCB for test chassis expected to arrive the week of 03/22/2021
5. Load PCBs have been manufactured and are on hand
6. Marc McMullen has the chassis and will cut a mounting hole for SAMTEC connector PCB

2. Hardware Interlock System development

Mary Ann Antonioli, Peter Bonneau, and Aaron Brown

1. Discussed Keysight switch and measurement unit and multiplexer
    - A LabVIEW program will be developed to control and monitor the Keysight switch and measurement unit and multiplexers
    - Questioned plastic that surrounds connector, preventing D-sub cable from securely connecting; will investigate installing a standoff on connector to allow a more secure connection
    - Additional set of two 50-pin, D-sub cables will be ordered

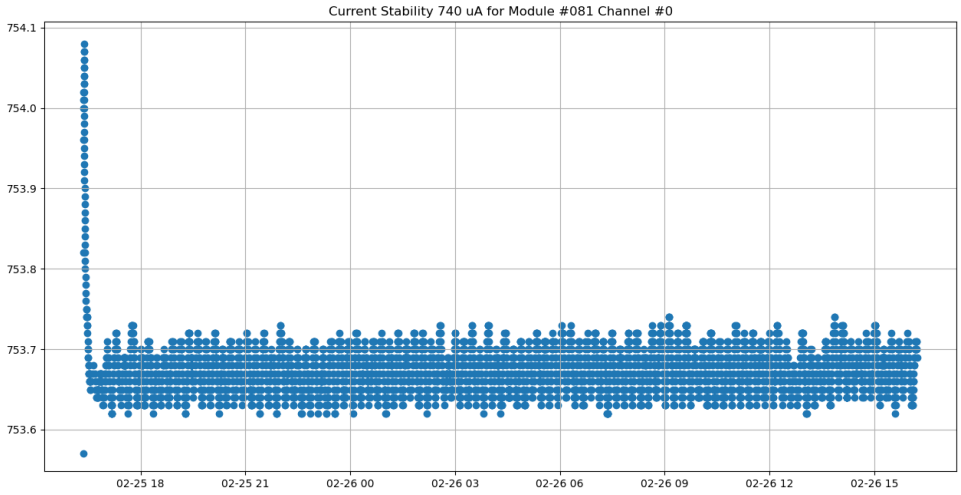


Left: Rear view of terminal block showing the plastic surrounding the connector. Right: Fifty-pin, D-sub connector with short thumb screws

3. Module Testing

Mary Ann Antonioli, Aaron Brown, and George Jacobs,

1. Reviewed voltage and current stability strip plots for module #081, channel 0



Voltage stability strip plot for A7435 module #081 channel #0

2. Mary Ann Antonioli will generate strip plots for all channels of all modules tested

4. V and I density plots

Aaron Brown and Brian Eng

1. George Jacobs will use Python program developed by Aaron Brown to generate density plots of the voltage and current stability test data for all channels of all A7030TN modules

5. **VME LED Driver (VLD) module slides**
   Mary Ann Antonioli and Aaron Brown
   1. Reviewed edited version of slides for VLD module manual *Section 1: Introduction*
   2. Reviewed slides for manual *Section 3: Functional Descriptions*
   3. Aaron Brown will discuss manual with Peter Bonneau and Brian Eng